ABSTRACT OF THE DISCLOSURE

A high performance single-pole-double-throw (SPDT) Transmitter/Receiver (T/R) FET switch utilizes a plurality of multi-gate FETs in series to realize low insertion loss, low harmonic distortion and high power handling capabilities. The SPDT switch consists of an antenna port, a transmitter branch coupled to a transmitter port through a plurality of multi-gate FETs in series and a receiver branch coupled to a receiver port through a plurality of multi-gate FETs in series. When a high power signal passes from the transmitter port to the antenna port through the transmitter branch, the receiver branch is required to be shut off electrically to prevent the high power signal from leaking to receiver port. This leakage can degrade the isolation of the switch and cause harmonic distortion. Furthermore, the transmitter branch is required to provide a resistance as small as possible to reduce the power loss when it passes through the transmitter branch to the antenna port. In the receiver branch, two of the gate metals in the multi-gate FETs are fabricated with gate sizes several times larger than the others. Furthermore, a heavily doped cap layer is utilized between the gate fingers in a multi-gate FET to reduce the channel resistance of FET, thereby lowering the insertion loss.